LIBRARY ieee ;

USE ieee.std\_logic\_1164.all ;

ENTITY lab6 IS

PORT ( x1,x2,x3 : in std\_logic;

f : out std\_logic);

END lab6 ;

ARCHITECTURE Behavior OF lab6 IS

BEGIN

f <= (NOT x1 AND NOT x2 AND NOT x3) OR (NOT x1 AND x2 AND NOT x3) OR (NOT x1 AND x2 AND x3) OR (x1 AND NOT x2 AND NOT x3) OR (x1 AND NOT x2 AND x3) OR (x1 AND x2 AND NOT x3);

END Behavior ;